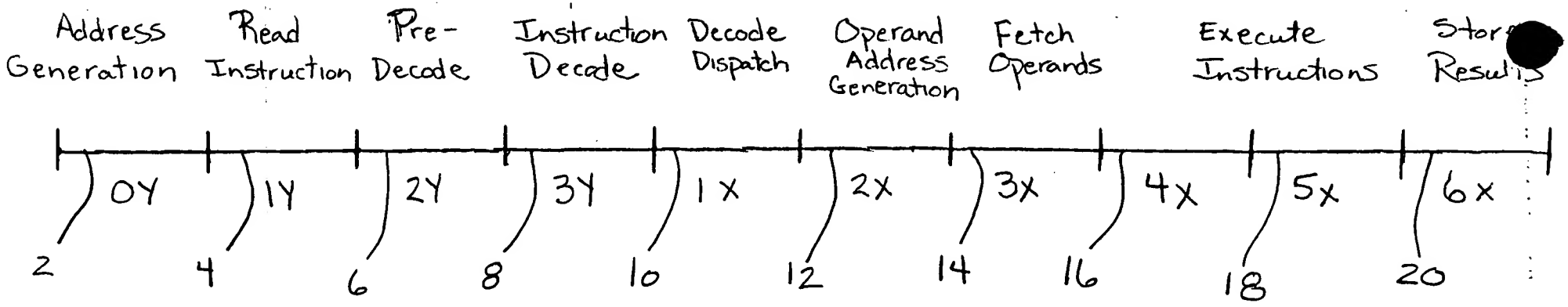
Address Generation
Read Instruction
Pre-Decode
Instruction Decode
Decode Dispatch
Operand Address Generation
Fetch Operands
Execute Instructions
Store Results
0Y
1Y
2Y
3Y
1X
2X
3X
4X
5X
6X
2
4
6
8
10
12
14
16
18
20

Figure 1

6602ET T5089n60

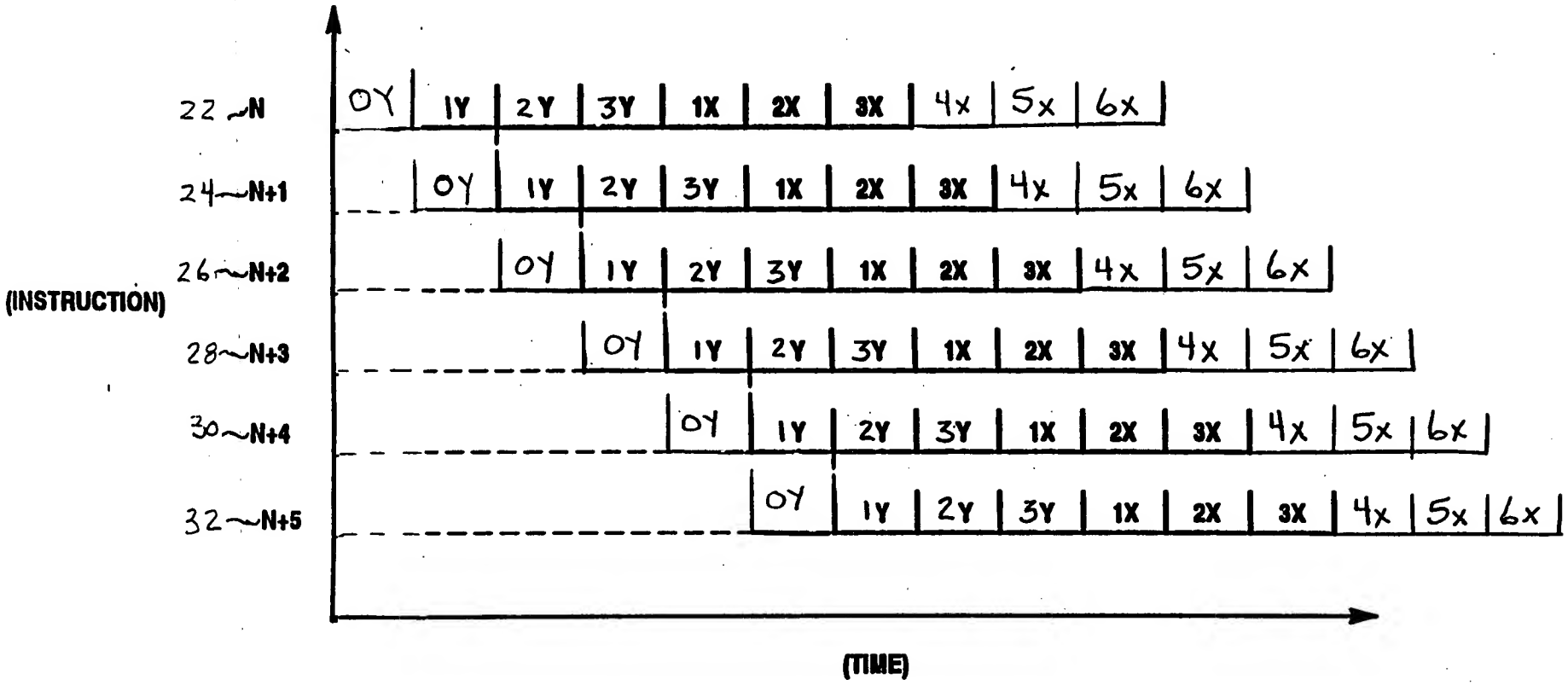

Figure 2

66021T T5089+60

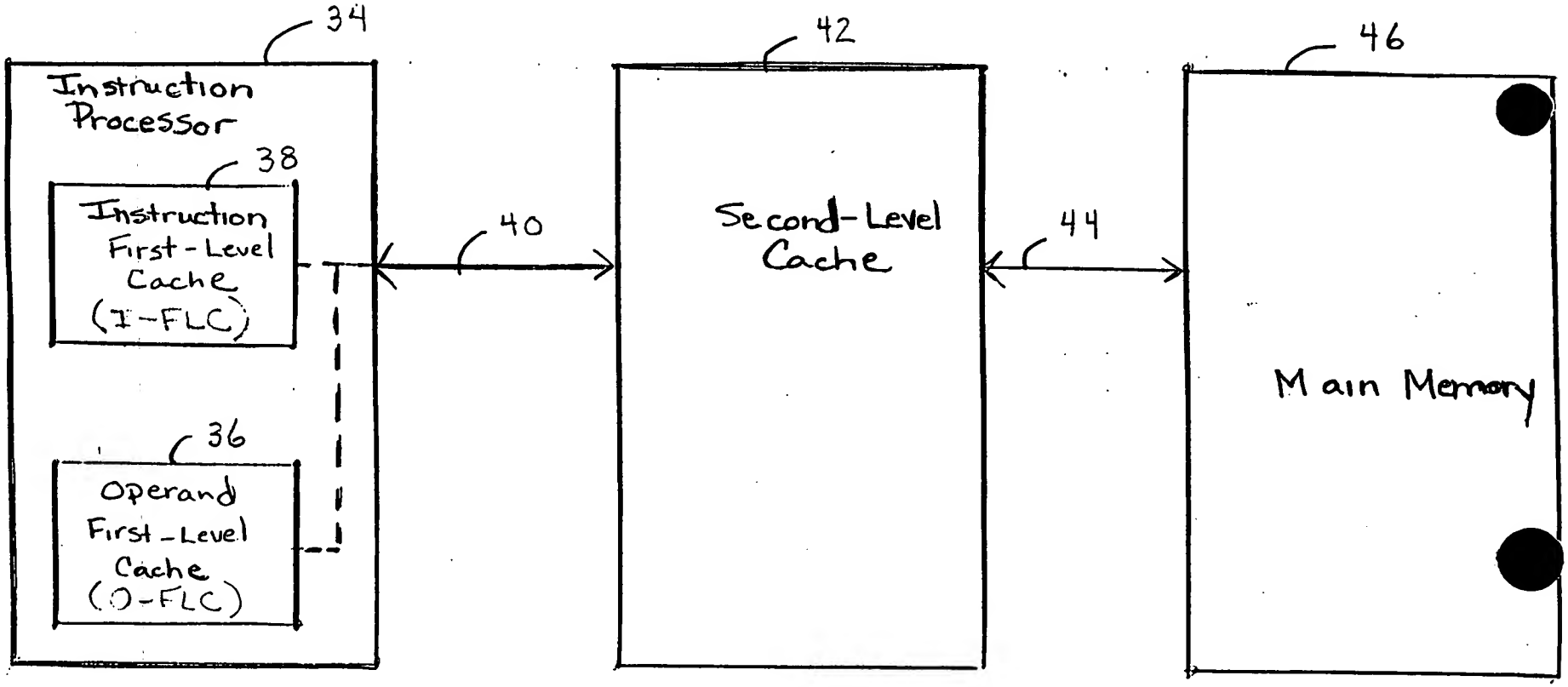

Figure 3

660227 T5089h60

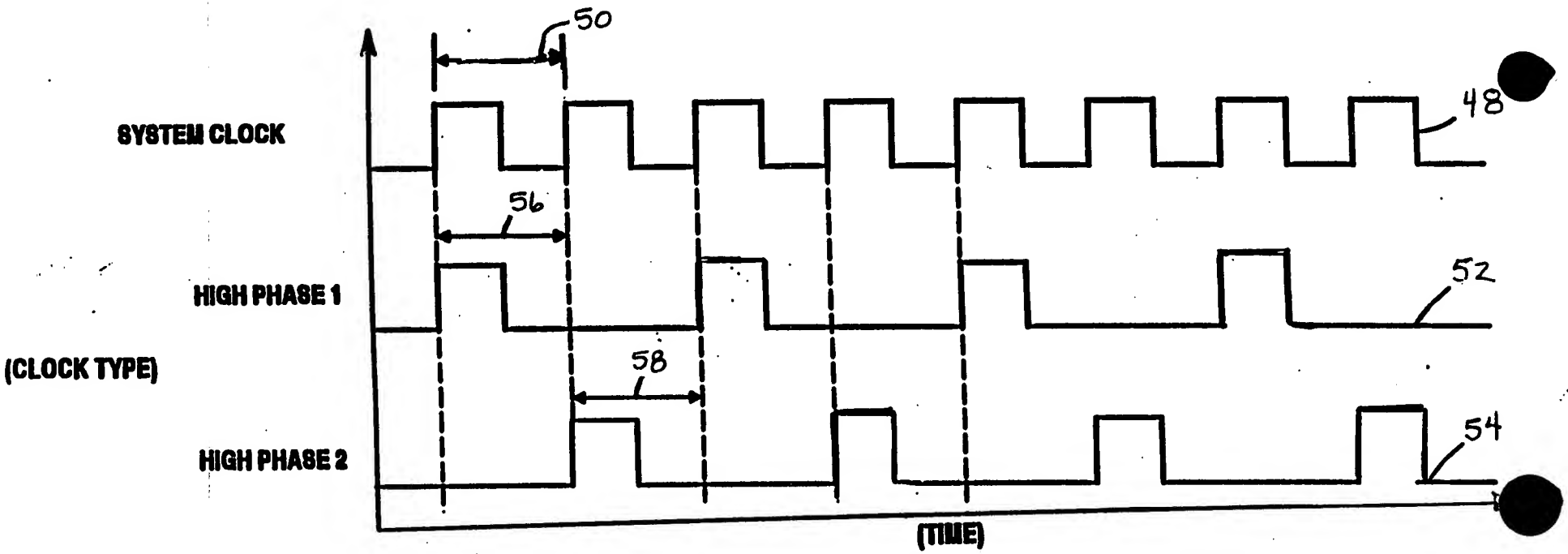

Figure 4

6602375 5089460

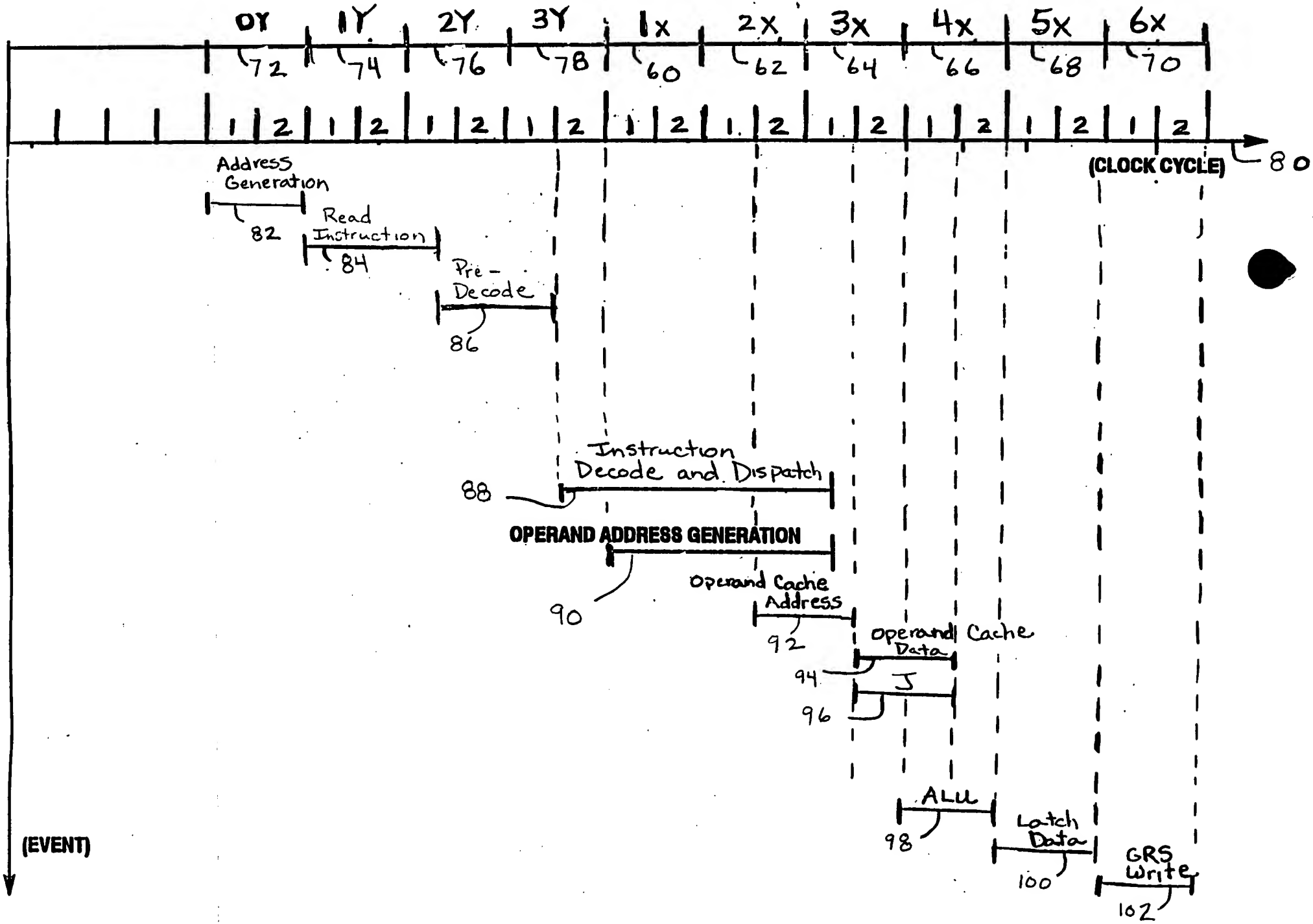

Figure 5

6602ET "T5089+60

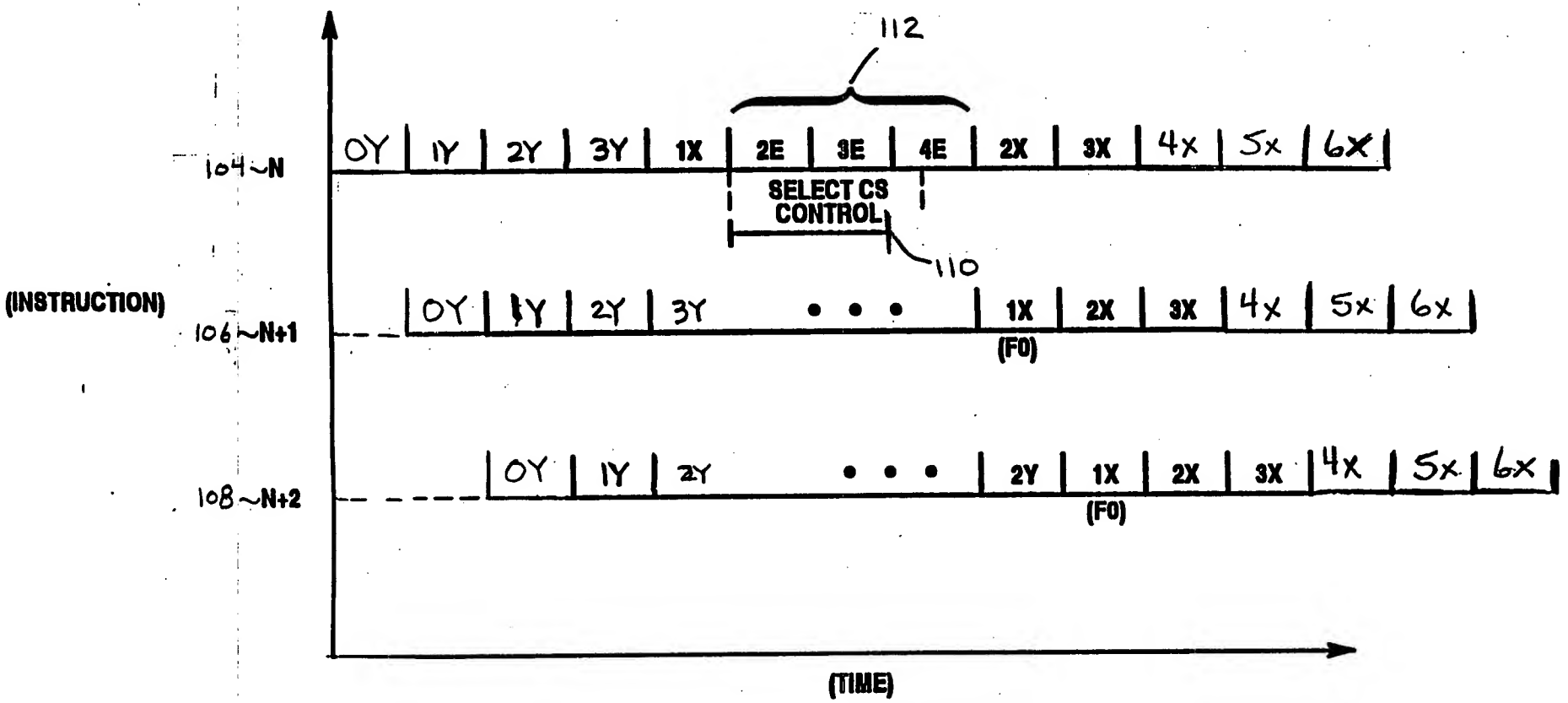

Figure 6

66022T "T5089h60

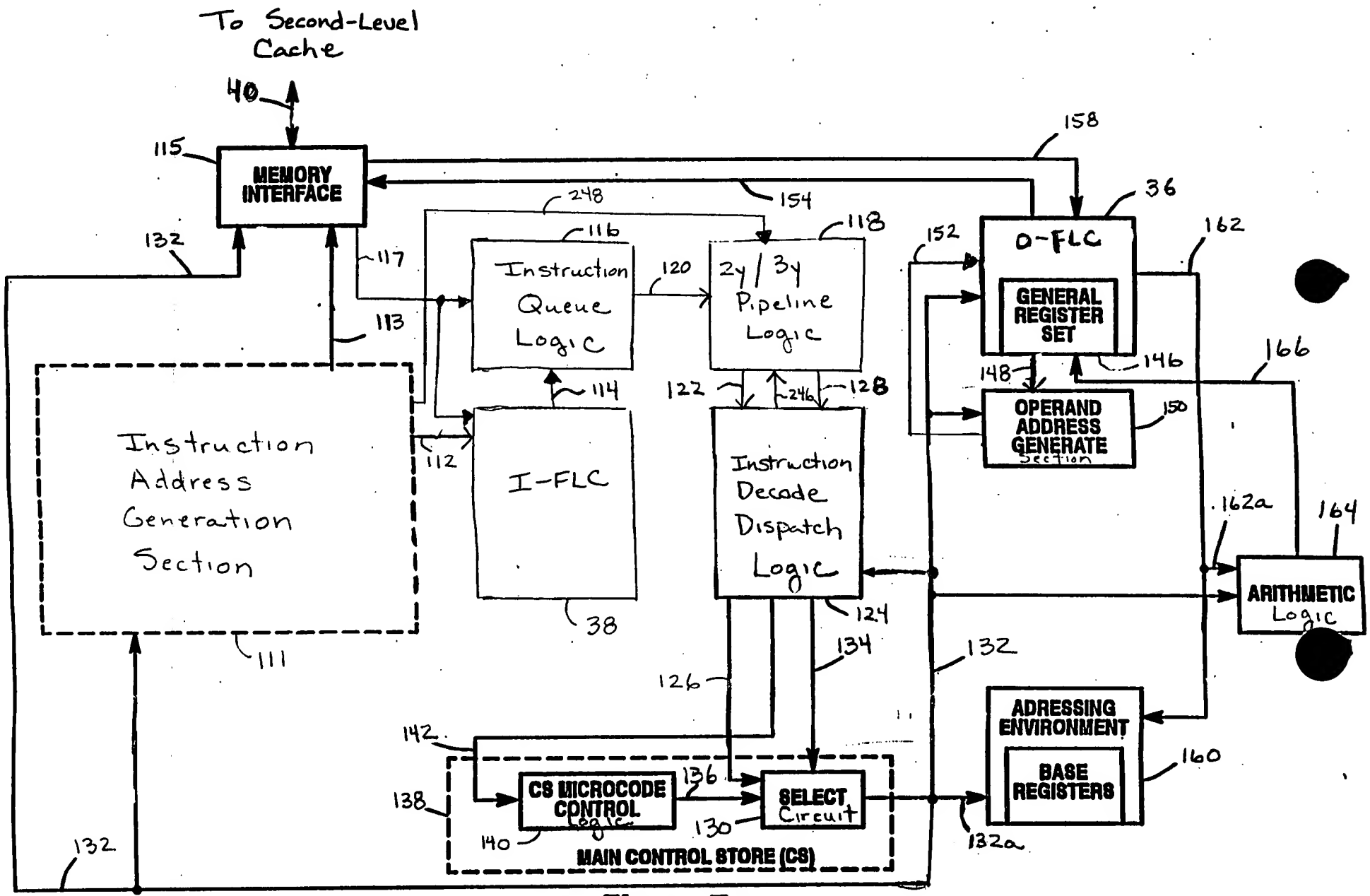

Figure 7

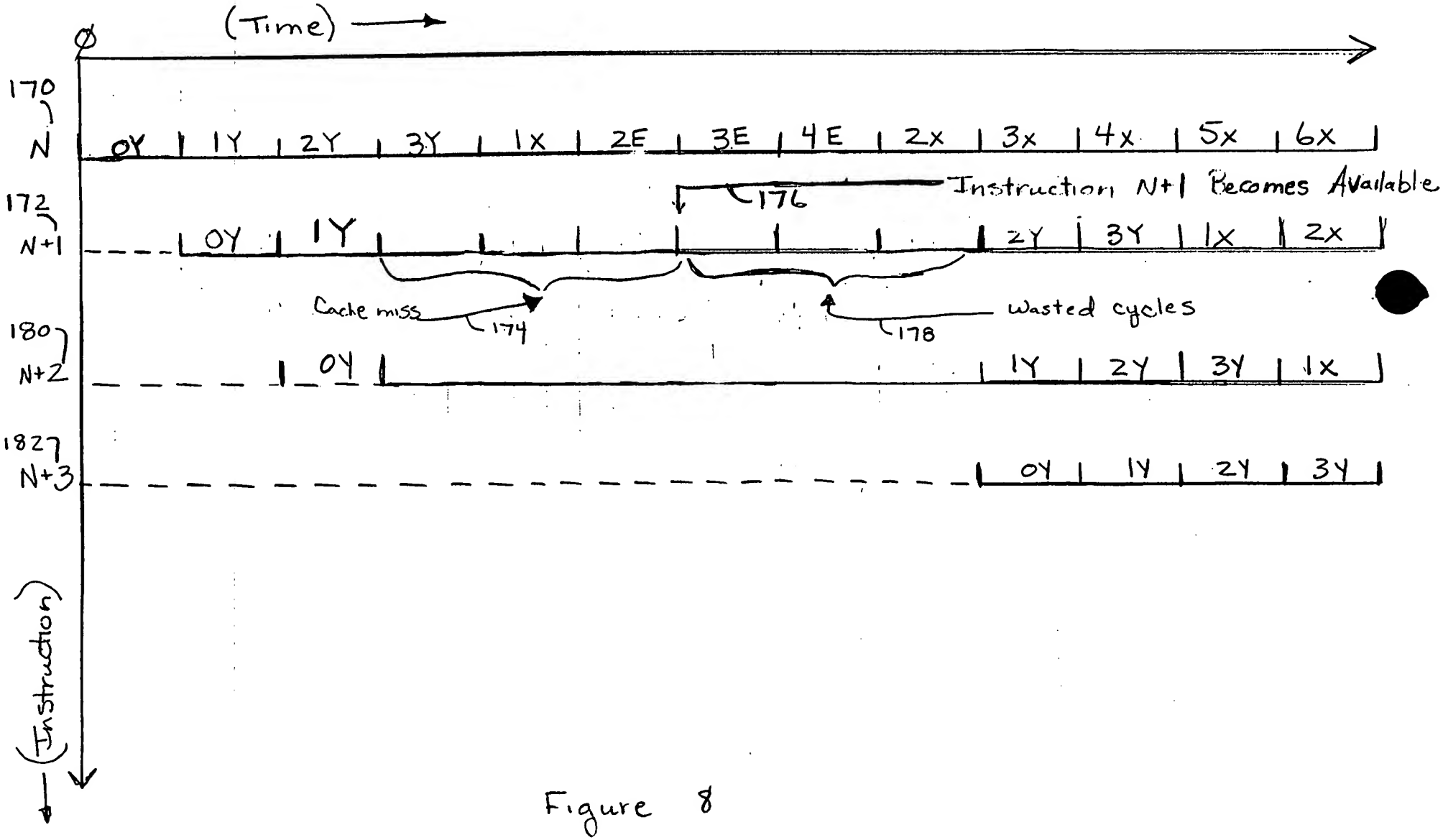
(Time)
0
170
N
0Y
1Y
2Y
3Y
1X
2E
3E
4E
2x
3x
4x
5x
6x
Instruction N+1 Becomes Available
176
172
N+1
0Y
1Y
2Y
3Y
1X
2x
Cache miss
174
wasted cycles
178
180
N+2
0Y
1Y
2Y
3Y
1X
182
N+3
0Y
1Y
2Y
3Y
(Instruction)

Figure 8

6602217 T5089M60

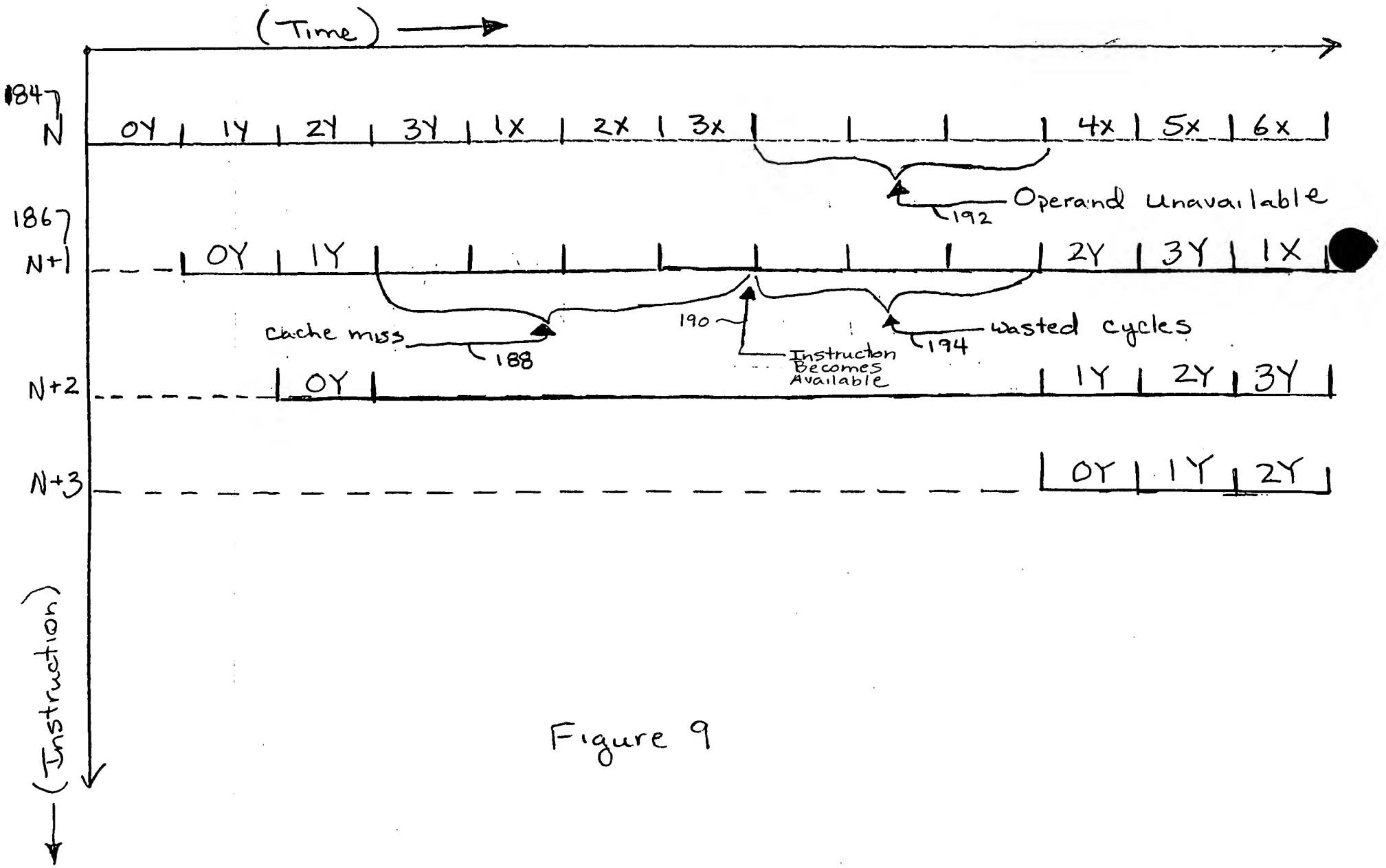

Figure 9

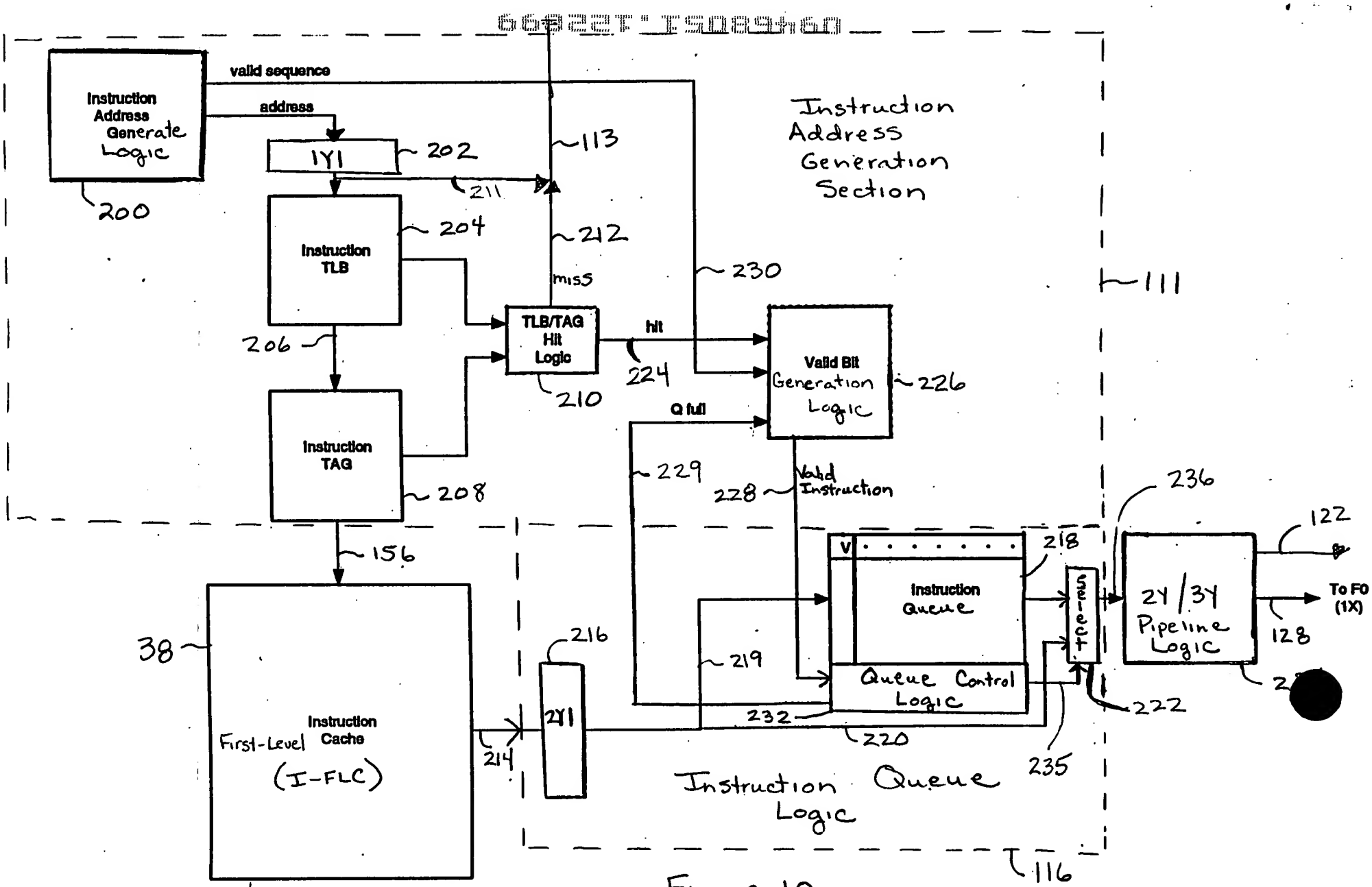
Instruction Address Generate Logic
valid sequence
address
200
IYI
202
211
113
Instruction TLB
204
206
212
miss
230
111
TLB/TAG Hit Logic
210
hit
224
Valid Bit Generation Logic
226
Q full
229
228
Valid Instruction
Instruction TAG
208
156
236
122
V
218
Instruction Queue
Select
2Y/3Y Pipeline Logic
To FO (1X)
128
38
216
219
Queue Control Logic
232
220
222
235
Instruction First-Level Cache (I-FLC)
214
241
Instruction Queue Logic
116

Figure 10

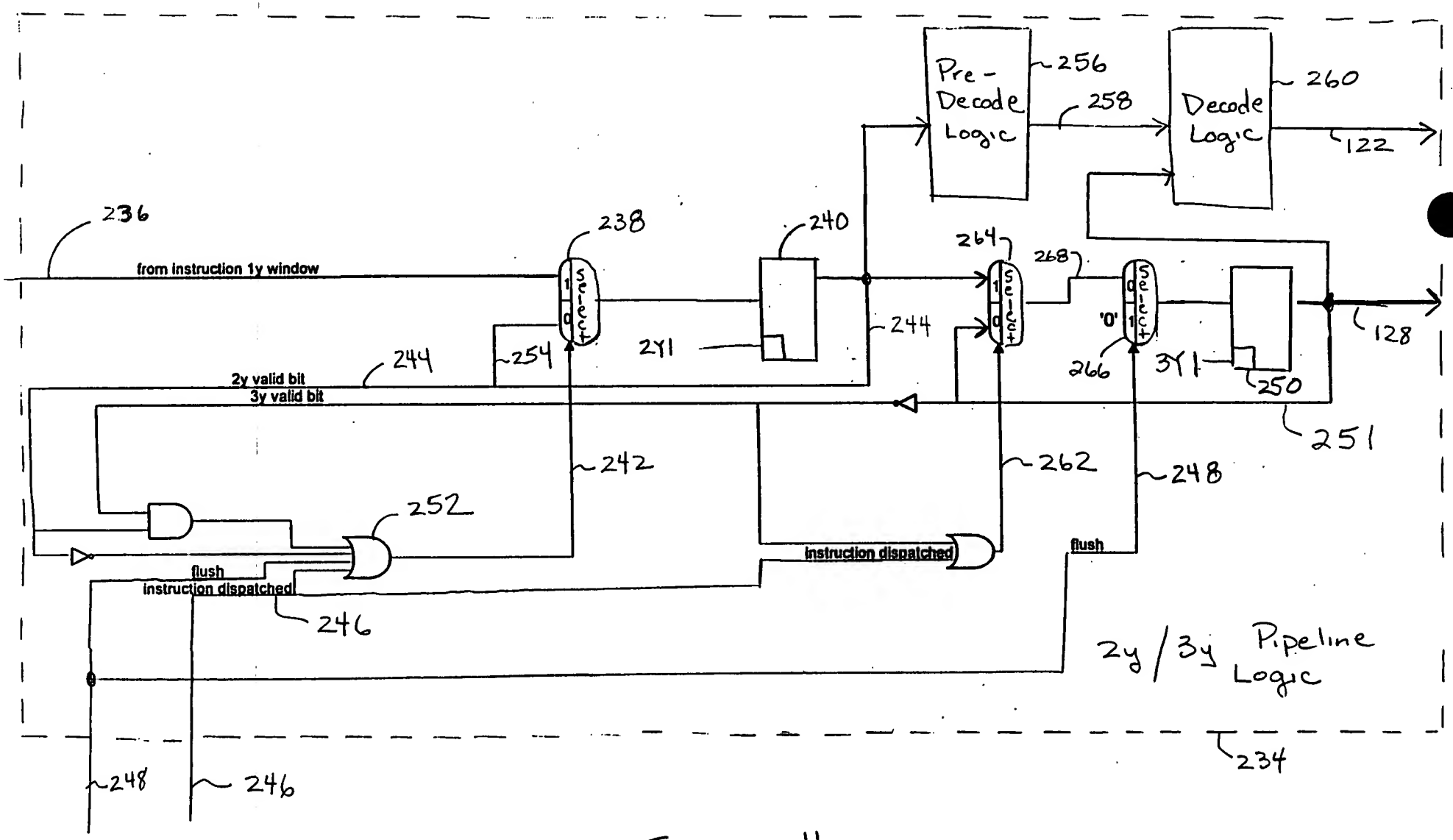
Pre-Decode Logic
256
Decode Logic
260
258
122
236
238
240
264
268
from instruction 1y window
Select
1
0
'0'
244
254
241
2y valid bit
3y valid bit
242
262
248
251
250
241
266
128
252
flush
instruction dispatched
246
instruction dispatched
flush
2y/3y Pipeline Logic
234
248
246

Figure 11

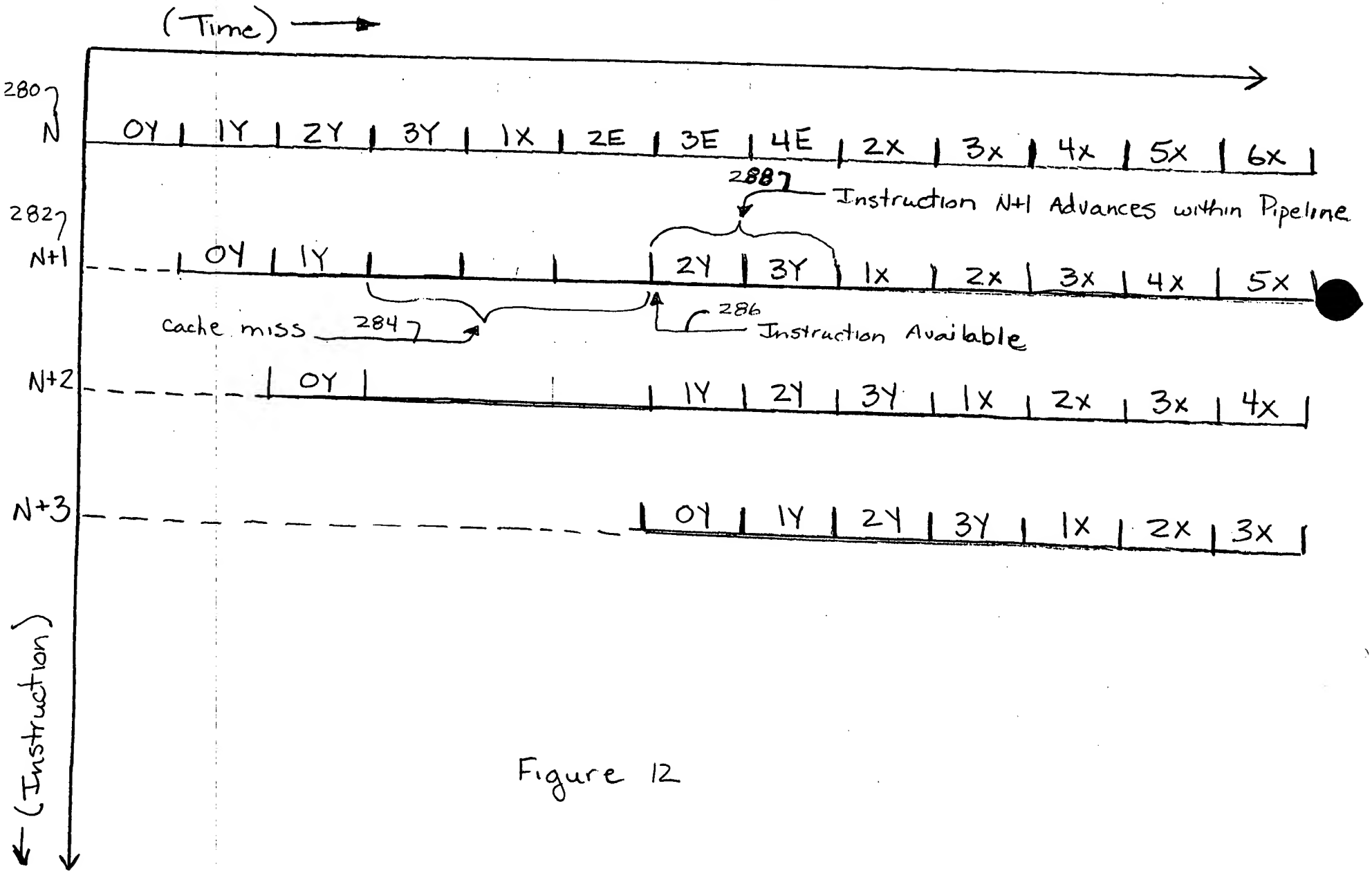
(Time)
280
N
0Y
1Y
2Y
3Y
1X
2E
3E
4E
2X
3X
4X
5X
6X
288
Instruction N+1 Advances within Pipeline
282
N+1
0Y
1Y
2Y
3Y
1X
2X
3X
4X
5X
cache miss
284
286
Instruction Available
N+2
0Y
1Y
2Y
3Y
1X
2X
3X
4X
N+3
0Y
1Y
2Y
3Y
1X
2X
3X
(Instruction)

Figure 12

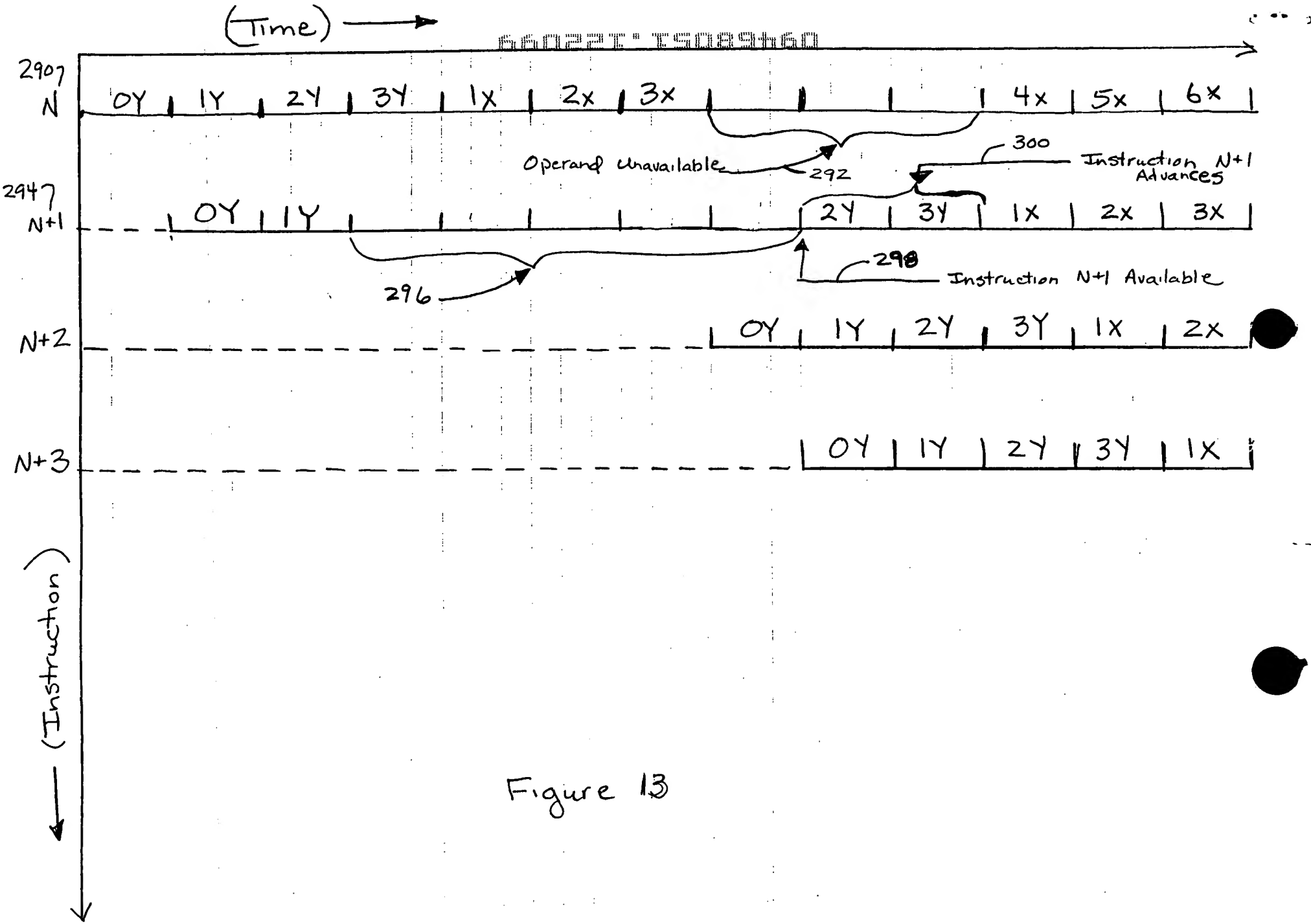
(Time)
2907
N
0Y
1Y
2Y
3Y
1X
2X
3X
4X
5X
6X
Operand Unavailable
292
300
Instruction N+1 Advances
2947
N+1
0Y
1Y
2Y
3Y
1X
2X
3X
296
298
Instruction N+1 Available
N+2
0Y
1Y
2Y
3Y
1X
2X
N+3
0Y
1Y
2Y
3Y
1X
(Instruction)

Figure 13